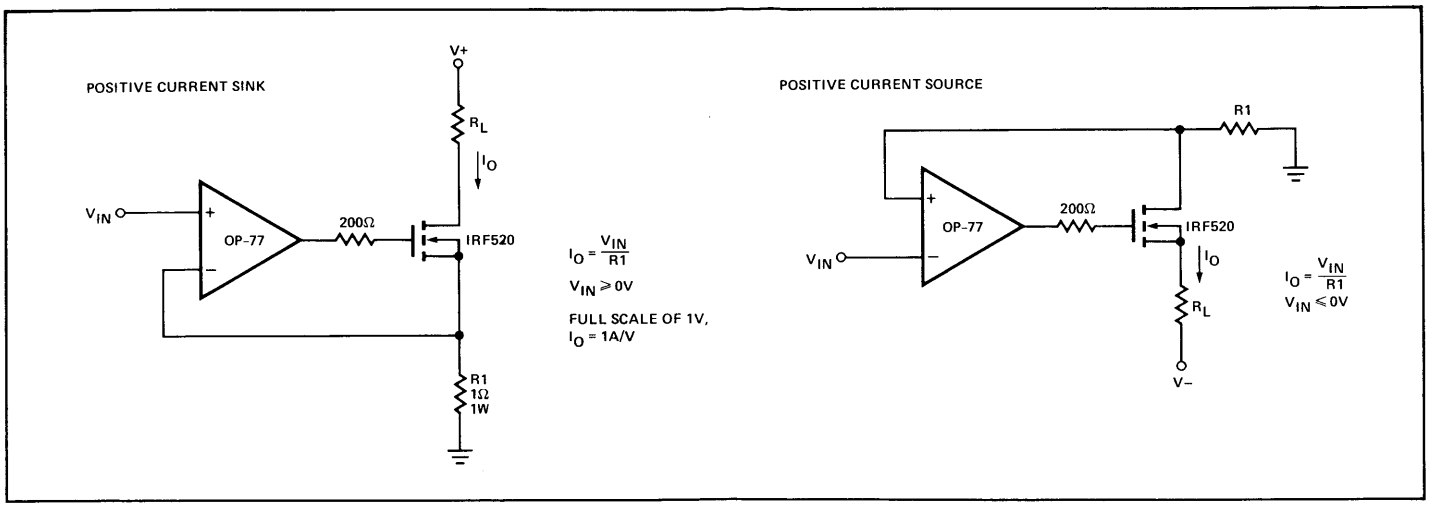
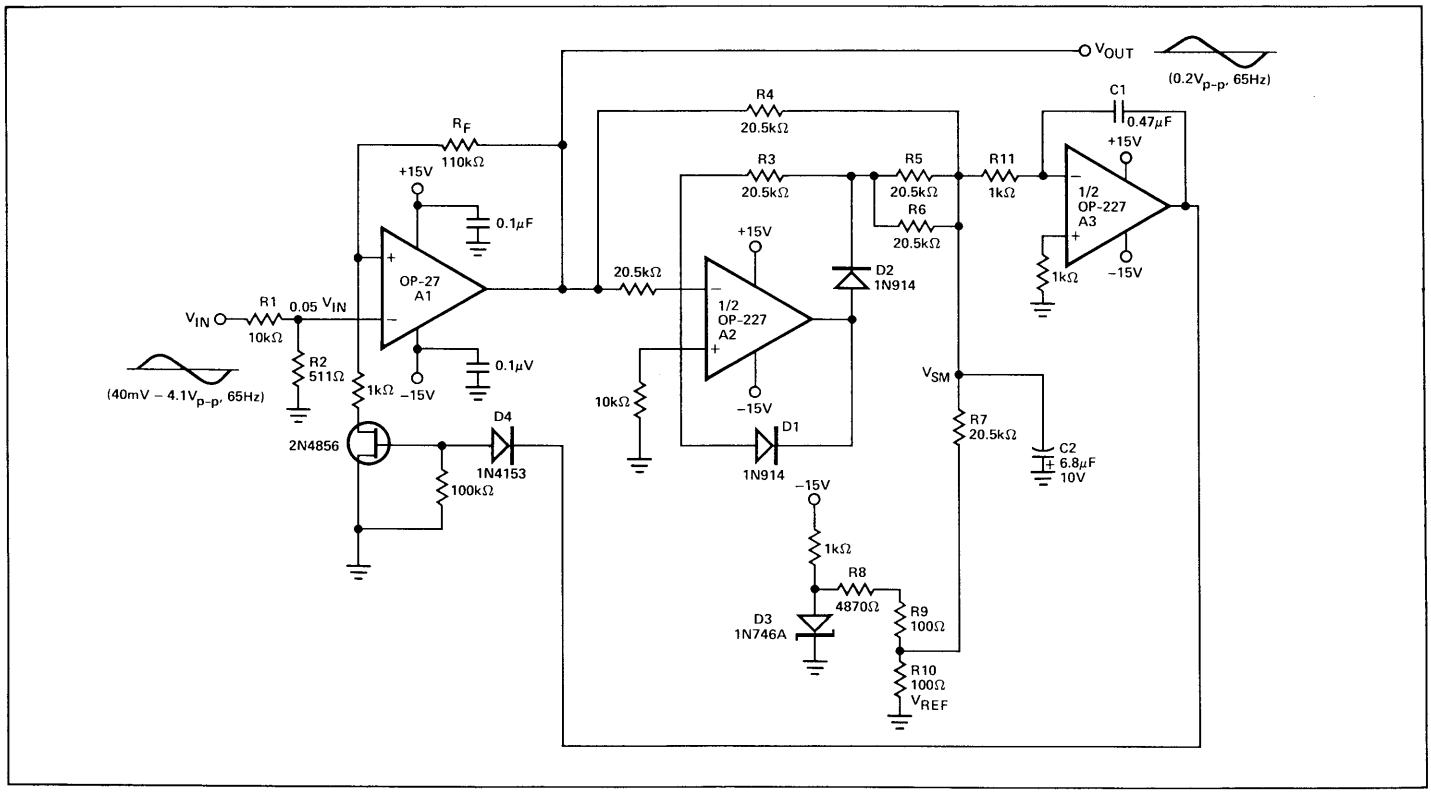
FIGURE 35: Precision Current Sinks



These simple high-current sinks require that the load float between the power supply and the sink. In these circuits, OP-77's high gain, high CMRR, and low TCV_{OS} assure high accuracy.

FIGURE 36: Low Noise AGC Amplifier



In this circuit, a JFET transistor is used to control the gain of the low-noise OP-27 amplifier over a two-decade input voltage range. For inputs from 40mV to 4.1V peak-to-peak, the AGC maintains a 0.2V peak-to-peak output.

Amplifier A2 performs an absolute-value operation on V_{OUT} and sums the result with a –0.2V reference on capaciator C2. The deviation of this sum, V_{SM}, from zero is amplified by A3 and controls the gate of the JFET. If the peak-to-peak amplitude of V_{OUT} exceeds 0.2V, V_{SM} becomes positive and drives the JFET gate negative. This increases the JFET's channel resistance lowering the gain of the A1. The reverse of this occurs if V_{OUT} falls below 0.2V peak-to-peak.

The values of C1 and C2 are chosen to optimize the circuits response time for a given input voltage frequency. This example was designed for a 65Hz signal. Higher frequencies would justify lower values for C1 and C2 to speed the AGC response.